ISSN 2348 – 9928
IJAICT Volume 4, Issue 12, December 2017 Doi:01.0401/ijaict.2015.10.02 Published on 05 (12) 2017

A LOW-COST, SYSTEMATIC METHODOLOGY FOR SOFT ERROR ROBUSTNESS OF LOGIC CIRCUITS

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Abstract—Due to current technology scaling trends such as shrinking feature sizes and decreasing supply voltages, circuit reliability is becoming more susceptible to radiation-induced transient faults (soft errors). Soft errors, which have been a great concern in memories, are now a main factor in reliability degradation of logic circuits as well. In this paper, present a systematic and integrated methodology for circuit robustness to soft errors. The proposed soft error rate (SER) reduction framework was based on redundancy addition and removal (RAR), which aims to eliminating those gates with large contribution to the overall SER. Several metrics and constraints are introduced to guide the RAR-based approach towards SER reduction. In this paper also integrate a resizing strategy as post-RAR additive SER optimization. The strategy can identify most critical gates to be upsized and thereby, minimize area and power overheads while maintaining a high level of soft error robustness. Experimental results show that the proposed RAR-based framework can achieve up to 70% reduction in output failure probability. On average, about 23% SER reduction is obtained with less than 4% area overhead.

Keywords— Gate Resizing, Redundancy Addition and Removal, Reliability, Soft Error Robustness, Soft Errors, Ser Rate. Single-Event Upset.

I INTRODUCTION

Circuit reliability has become a critical issue in the deep submicrometer design era. Crosstalk, voltage drop, and radiation-induced transient errors are currently some of the main factors in reliability degradation. Due to current technology scaling trends (encompassing shrinking feature sizes, lower supply voltages, smaller node capacitances, etc.), digital designs are becoming more susceptible to radiation-induced particle hits resulting from radioactive decay and cosmic rays, than all other factors. A low energy particle that before had no effect on a circuit cans now flip the state of a storage node. Such a bit-flip of a node is called a singleevent transient (SET) or a glitch. A single-event upset (SEU) or a soft error occurs if the SET is propagated to an output and latched into a memory element. The rate at which soft errors occur is called soft error rate (SER). During SET propagation, the following three mechanisms used to provide logic circuits with effective protection against soft errors.

1) Logical Masking: *A* SET which is not on a sensitized path from the location where it originates is logically masked.Once a SET is logically masked, it no longer has any influence on the target circuit; i.e ., both of its amplitude and duration become zero [1][2].

2) Electrical Masking: ASET which is attenuated and becomes too small in amplitude or duration to be latched is electrically masked. While a SET may be latched if its attenuated amplitude and durtion are still large enough, electrical masking can reduce the overall impact of SETs.

3) Latching-Window Masking: A SET which does not arrive "on time" is also masked, depending on the setup and hold times of the target memory element. The basic condition for a SET to be latched is to have its duration greater than the sum of setup and hold times and to reach the memory element during the latching window[3].

These three mechanisms prevent some SETs from being latched and alleviate the effects of soft errors in digital systems. However, continuous scaling trends have negative impact on these masking mechanisms. Decreasing logic depth in super-pipeline stages reduces the probability of logical masking since the path from where a SET originates to a latch is more easily sensitized. The pulse attenuation because of electrical masking, determined by gate delay, also decreases due to smaller contribution of gate delay compared to wire delay. Higher clock frequencies increase the number of latching windows per unit of time and thus facilitate SET latching. As a result, soft errors in logic become as great of a concern as in memories, where soft errors can be mitigated by conventional error detecting and correcting codes[4][5].

II SER REDUCTION

We develop a systematic SER reduction framework using redundancy addition and removal (RAR) and integrate a gate

resizing strategy for soft error robustness into the proposed framework. RAR has been presented as a successful logic optimization technique which iteratively adds and removes redundant wires to minimize a circuit in terms of literal count or clock period. Since during each step of wire addition and removal the soft error rate of a circuit may vary, we rely on estimating the effects of redundancy manipulations and accept only those with positive impact. The new resizing strategy focuses on identifying gates that are truly most critical and discarding gate that are not required to be resized. The end result of such an integrated methodology is a net reduction in soft error rate. The proposed framework has the following several advantages and contributions over other existing techniques.

First, our RAR-based approach undergoes very little area over head since there usually exists one or more redundant removable wires after a redundant wire is added into a circuit. Also, because of the efficiency in run time and memory usage of the RAR algorithm, our idea of redundancy identification and manipulation for[6][7] SER reduction can be applied effectively to large circuits. Then, our framework trust on a symbolic reliability analyzer which provides a unified treatment of three masking mechanisms through decision diagrams. Hence, all masking mechanisms are considered jointly as criteria for SER reduction. Also, we introduce a novel metric for masking impact analysis. Using this metric, a systematic algorithm, which can precisely estimate the impact on SER of an added/removed wire and decide whether to accept the given addition/removal step in RAR, is developed. Finally, such an approach is orthogonal to existing techniques targeting gate resizing and flip-flop selection; they are thus equilibrium to provide additive savings on top of our framework. In this paper, we demonstrate the effectiveness of gate resizing integrated with our framework as post RAR SER optimization. The proposed strategy picks most critical gates to be upsized and is effective in reducing area and power overheads.

III SER ANALYSIS

Analyzing the soft error rate of a circuit accurately and efficiently is a crucial step for SER reduction. Intensive research has been done so far in the area of SER modeling and analysis. Among various existing modeling frameworks, we choose the symbolic one presented as the SER analysis engine. We motivate our choice by the fact that, by using this symbolic SER analyzer, we can simultaneously quantify the error impact and the masking impact of each gate in combinational logic.

Terminal node "0" of the ADD associated with a gate represents all cases where a glitch is logically or electrically masked, other terminal nodes represent the remaining values for duration or amplitude after a glitch passes through a gate. The initial ADD of each gate is built for the glitch originating at that gate. It consists of only one terminal node initial duration or amplitude value. These initial ADDs are propagated to respective fan-out gates, which use them to create new ADDs based on the attenuation [8][9]model and related sensitization BDDs. Sensitization BDDs include information about logical masking. The sensitization BDD of gate G to gate G' is just the Boolean difference of G' with respect to G. Input vectors that make the sensitization BDD of path G to G' go to terminal node "0" logically mask glitches from gate G at gate G'. Therefore, only paths ending up in terminal node "1" of the sensitization BDD and a node different from "0" of the associated ADD, need to be considered for calculating new values relying on the attenuation model. All other cases, which indicate either logical or electrical masking, go to terminal node "0". Fig. 2 demonstrates the overall process of building duration ADDs for a glitch originating at gate G_2 Fig.1.

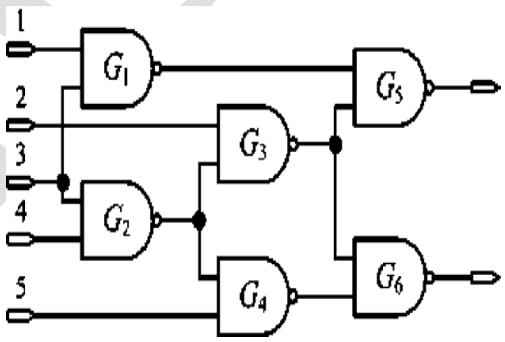

Fig 1 : MCNC'91 Benchmark Suite.

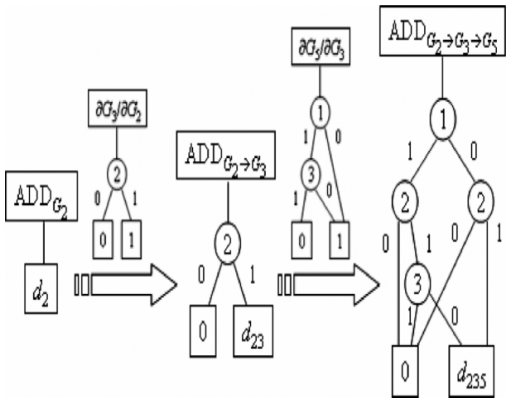

Fig 2: Duration ADDs for a glitch Originating at gate G_2, and Passing through gate G_3 and G_5

ISSN 2348 – 9928
Doi:01.0401/ijaict.2015.10.02 Published on 05 (12) 2017

3.1 RAR based approach for SER reduction

In this section, we present SER reduction approach based on redundancy addition and removal (RAR). RAR is a logic minimization technique which performs a series of wire/gate addition and removal operations by searching for redundant wires/ gates in a circuit. Wires for addition can be identified according to the mandatory assignments made during automatic test pattern generation (ATPG). For our objective of SER reduction, using redundancy addition and removal in an unsystematic manner may increase SER by reducing the number of gates or the depth of circuits: a smaller gate count will affect the impact of logical masking, while smaller logic depth will reduce the impact of both logical and electrical masking. The basic principle of our proposed framework is to keep wires/gates with high masking impact and to remove wires/gates with high error impact. Mean masking impact (MMI) and mean error impact (MEI), used as key metrics for guiding the RAR-based approach[10][11].

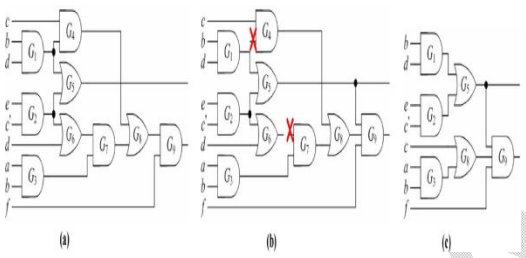

Fig 3 : (a) The original circuit.
(b) The circuit after redundancy addition
(c) The circuit after redundancy removal

3.2 Mean Error Impact (MEI)

For each internal gate G_i, initial duration d and initial amplitude a, MEI over all primary outputs F_j that are affected by a glitch occurring at the output of gate is defined as,

$$MEI\left(G_i^{d,a}\right) = \frac{\sum_{k=1,j=1}^{nf,nF} P\left(\left\{F_j\ fails \middle| G_i fails \bigcap \text{init}_{\text{glitch}}=(d,a)\right\}\right)}{n_F.n_F}$$

Where, n_f is the cardinality of the set of primary outputs in the circuitF_j , and n_F is the cardinality of the set of probability distributions f_k. The MEI value of a gate quantifies the probability that at least one primary output is affected by a glitch originating at this gate. The larger MEI a gate has, the higher the probability that a glitch occurring at this gate will be latched. This implies that those gates with higher MEI make the circuit more vulnerable to soft errors. Thus, it is benificial for SER if gates with large MEI are removed from the circuit.

3.3 Mean Masking Impact

we define mean masking impact on duration as,

$$MMI_D\left(G_i^{d,a}\right) = \sum_{k=1}^{n_f}\sum_{j=1}^{n_G} MI_D\left(G_j^{d,a} \rightarrow G_i\right)$$

Where n_G is the cardinality of $C(G_i)$,n_f is the cardinality of the set of probability distributions (f_k) and $\left(G_j^{d,a} \rightarrow G_i\right)$ masking impact on duration of gate G_i with respect to gate G_j , denotes the absolute duration attenuation contributed by gate G_i on a glitch with duration 'd' and amplitude 'a'originating at gate G_j.The overall algorithm of our RAR based approach is given below,

```
00 RAR-based SER reduction (circuit, T1, T2, T3, T4, T5) {
01   Compute MEI and MMID for each internal gate in circuit;
02   while (pair of candidate wires wa and wr identified by RAR) {
       // where wa is for addition and wr is for removal.
       // Constraint 4: topology constraint, applied first
03     s ← source gate of wire wa;
04     t ← destination gate of wire wa;
05     u ← source gate of wire wr;
06     v ← destination gate of wire wr;
07     if (gate t is not a dominator of both gate u and gate v)
08       goto notDominator;
09     if (wires wa and wr performed for SER reduction, based on (12) (14)) {
10       Add wa into circuit;
11       Remove wr from circuit;
12       continue;
       }
13   notDominator:
       // Wire addition procedure
14     if ((MEI(t) >= T1) || (MMID(t) <= T2)) continue; // Constraint 1
15     Add wa into circuit;
       // Wire removal procedure
16     gain ← 0;
17     sorted_wires ← Sort all removable wires due to the addition of wa
         by the MEI values of their source gates, from the largest to smallest;
18     for each (wire wr' in sorted_wires) {
19       if (wire wr' is no longer redundant) continue;
20       u ← source gate of wire wr';
21       v ← destination gate of wire wr';
22       if ((MEI(v) <= T3) || (MMID(v) >= T4)) continue; // Constraint 2
23       if (P(gate u goes to cv(v)) >= T5) continue; // Constraint 3
24       Remove wr' from circuit;
25       gain ← gain + 1;
       }
26     if ((gain > 0) || (MEI(t) is extremely small))
27       Keep wa in circuit;
28     else
29       Remove wa from circuit;
30     Update MEI and MMID for affected gates;
     }
   }
```

The proposed RAR-based approach is considered as a logic/gate-level optimization methodology for SER reduction. The main idea for reducing circuit SER is by increasing the effects of logical masking and electrical masking.

IV EXPERIMENTAL RESULT

We have implemented the RAR-based SER reduction framework in and conducted experiments on a set of benchmarks from ISCAS'85 and MCNC'91 suites. The technology used is 70 nm PTM. The clock period used for probability computation is 250 ps, and setup and hold times for output latches are both assumed to be 15 ps. The supply voltage is set to be 1 V. To calculate SER the allowed intervals for initial duration are assumed to be 60ps and 120ps and amplitude are assumes to be 0.8V and 1V.The below table shows the overall performance of the SER reduction and MES improvement.

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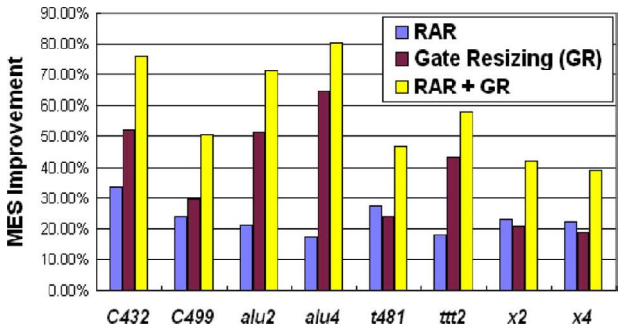

Fig 4 : SER-Aware Optimization

The blue color indicates the proposed RAR-based approach and the purple color indicates the gate resizing strategy and the yellow color indicates the integrated RAR and gate resizing methodology .

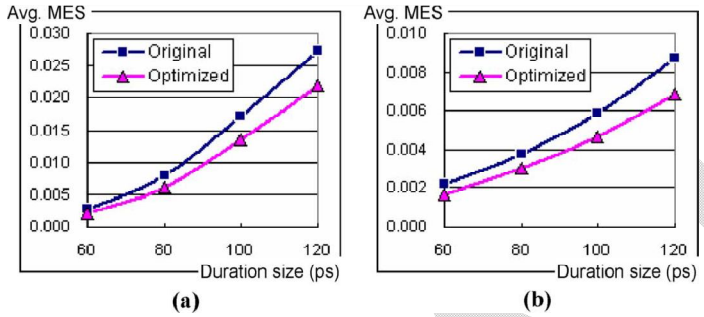

Fig 5 : Output for MES improvement

V CONCLUSION

In this paper, we propose a RAR-based ser reduction framework for combinational circuit. Two metrics, MEI and MMI, are used for efficient estimation of ser changes during RAR iterations. This methodology is easily applicable to sequential circuits in conjunction with an accurate and efficient ser analyzer for sequential circuits. Furthermore, a gate resizing strategy is integrated as a post-RAR procedure to provide additive SER improvement

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